REMARKS

This Response seeks to place this application in condition for allowance. Claims 1-41 are pending. All of the Examiner's rejections have been addressed. Some of the pending claims have been amended. No new matter has been added.

Amendments to the Claims

Applicants have made non-substantive amendments to some of the claims to retain consistency of claim terms between the dependent claims and the corresponding independent claim, to correct for obvious errors that are non-substantive in nature, improve antecedence of the claim language and/or improve the clarity of these claims. Applicants have also amended claims 12 and 26 to more particularly point out the claimed subject matter as is discussed below. No new matter has been added.

OFFICE ACTION

In the Office Action mailed April 5, 2002 (hereinafter, the "OFFICE ACTION"), claims 15, 19-20, and 35-36 were rejected under 35 USC 112, first paragraph, claims 12 and 26 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 5,173,878 to Sakui et al., (hereinafter, "Sakui"), and independent claims 12 and 26 and certain dependent claims were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 4,243,703 to Farmwald et al., (hereinafter, "Farmwald").

Finally, claims 1-11 are allowed. The rejections are addressed separately below.

35 USC 112 Rejection

In the OFFICE ACTION, claims 15, 19-20 and 35-36 were rejected under 35 USC 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the OFFICE ACTION (on page 2, items 2.1-2.3) states:

> 2.1. For claims 15 and 29: the claimed limitation of "wherein the first column address and the first row address are both included in a first packet, and the second column address and the page mode information is included in a second packet" is not supported by the original disclosure.
>
> 2.2. As per claims 19 and 35: the original disclosure does not support the claimed limitation of "wherein the first column address is received during a first clock cycle and the and the first row address is received during a second clock cycle". There is no disclosure of the relationship between the clock cycles and the bus cycles [e.g., bus cycles in figures 3 and 4].
>
> 2.3. As per claims 20 and 36: the original disclosure does not support the claimed limitation of "a first portion of the first column address is received during a first bus cycle and a second portion of the first column address is received during a second bus cycle, and wherein both the first and the second bus cycles transpire during the first clock cycle".

These rejections are addressed below individually.

Claims 15 and 29 are Fully Supported by the Specification

Claims 15 and 29 each recite, in part, "... the first column address and the first row address are both included in a first packet, and the second column address and the page mode information are included in a second packet." Applicants submit that claims 15 and 29 are fully supported by the specification.

In an embodiment, a memory device receives a packet and "... processes the information

received to determine the type of memory request, the address of the memory request and the number of bytes of the transaction." (see page 6, lines 17-19) Here, the address includes a column address and a row address, see for example, page 6, lines 21-24, "The memory address consists of the row address which is used during the row address strobe (RAS) in the DRAM and the column address which is used during the column address strobe (CAS) in the DRAM." In an embodiment, a packet includes page mode information, in addition to the column address, for example, page 8 lines 1-15 and Fig. 3:

> As the lower bits of the memory address are placed in the first two words of the packet... op code bits, op[3:0], which identify the type of access to be performed (e.g., page mode access)... are transmitted within the first 4 words of the packet, coincident with the transmission of the memory address. Preferably the memory operation types are coded in such a manner that the bits of the memory address indicate whether a page mode memory operation is to be performed.

Thus, in accordance with one or more embodiments, a first packet includes a row address and a column address and a second packet includes a column address and page mode information[1], since multiple packets received by the memory device may include each of a row address, a column address and page mode information.

Claims 19 and 35 are Fully Supported by the Specification

[1] In an embodiment, "page mode" indicates that locations in a common row are accessed using separate requests, see for example page 6, line 25 to page 7, line 3, i.e., "When operable in page mode, if a subsequent request to access data is directed to the same row, the DRAM does not need to wait for receipt of the row address and to assert RAS, as RAS has been asserted during the previous memory access. Thus, the access time for this data is shortened."

Claim 19 recites, in part " ...first column address is received during a first clock cycle and the first row address is received during a second clock cycle", while claim 35 recites in part "... the first column address is issued during a first clock cycle, and the first row address is issued during a second clock cycle".

Applicants submit that Claims 19 and 35 are fully supported by the specification. In the exemplary embodiments illustrated in figures 3 and 4, every two "bus cycles" correlate to a single clock cycle of a clock signal, for example, "Count Bits [7:2]" (i.e., Count bits [6,4,2] transmitted during bus cycle 4, and Count Bits [7,5,3] transmitted during bus cycle 5) are received by the memory device during one clock cycle. See page 12, lines 25-26 of the specification, i.e., "...count bits [7:2] are transmitted across the bus during one clock cycle...". Thus, two bus cycles (e.g., "bus cycles 4 and 5", figs. 3 and 4) transpire during a single clock cycle.

Claims 20 and 36 are Fully Supported by the Specification

Claim 20 recites in part, "... a first portion of the first column address is received during a first bus cycle and a second portion of the first column address is received during a second bus cycle, ... both the first and second bus cycles transpire during the first clock cycle." Claim 36 recites in part, "... a first portion of the first column address is issued during a first bus cycle and a second portion of the first column address is issued during a second bus cycle... both the first and second bus cycles transpire during the first clock cycle." Applicants submit that claims 20 and 36 are fully supported by the specification of the instant application as filed.

In an embodiment, a memory device will "... use the lower order portion of the memory address as the column address bits", (page 7, lines 10-11), and "... the lower order bits of the memory address are placed in the first two words of the packet." In the embodiment, each word of the packet

is transmitted during a single bus cycle, two of which transpire during each clock cycle as was explained above with respect to claims 19 and 35, (e.g., see page 12, lines 25-26 of the specification and figs 3 and 4).

35 USC 102(e) Rejections

Independent claims 12 and 26 were rejected under 35 USC 102(e) as being anticipated by Sakui. In addition, independent claims 12 and 26 and certain dependent claims (OFFICE ACTION, page 3, item 4) were also rejected under 35 USC 102(e) as being anticipated by Farmwald. Applicants have amended independent claims 12 and 26 to more particularly point out and claim the subject matter.

In particular, Applicants have amended claim 12 to additionally include, in part:

> receiving first operation code information during a first clock cycle of an external clock signal;
> receiving second operation code information successively after receiving the first operation code information...
> wherein data stored in the first memory cell is accessed for a memory operation based at least in part on the first and second operation code information.

No new matter has been added and the amendment to claim 12 is fully supported in the specification, for example, see page 6, line 12 to page 8, line 15. Applicants submit that neither Sakui or Farmwald disclose or describe receiving first operation code information during a first clock cycle of an external clock signal, receiving second operation code information successively after receiving the first operation code information and data stored in the first memory cell being accessed for a memory operation based at least in part on the first and second operation code information.

In addition claim 26 has been amended to recite, in part:

> issuing first operation code information during a first clock cycle of an external clock signal;
> issuing second operation code information successively after issuing the first operation code information... wherein data stored in a location is accessed for a memory operation based at least in part on the first and second operation code information.

No new matter has been added and the amendment to claim 26 is fully supported in the specification, for example, see page 6, line 26 to page 8, line 15. Applicants submit that neither Sakui or Farmwald disclose or describe issuing first operation code information during a first clock cycle of an external clock signal, issuing second operation code information successively after issuing the first operation code information and data stored in a memory cell located at the location being accessed for a memory operation based at least in part on the first and second operation code information.

Thus, independent claims 12 and 26 (and the dependent claims which incorporate the limitations of the base claims) are not anticipated by either Sakui or Farmwald. It should be noted although not separately addressed herein, dependent claims 13, 14, 16-18, 21-23, 27, 28, 30-34, and 37-39 incorporate limitations that present patentable subject matter in their own right. In short, these limitations are also not disclosed (inherently or otherwise) or employed in either Sakui or Farmwald.

It should be noted that Applicants amendment of independent claims 12 and 26 is not to be construed as an admission that Applicants agree in any way with the rejections based on Sakui or Farmwald. Indeed, no inference or conclusion of any kind should be drawn from the absence of comments pertaining to certain limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks and amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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